



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,790	03/26/2004	Hooman Honary	1020.P18416	5212
57035	7590	03/14/2007	EXAMINER	
KACVINSKY LLC			LI, AIMEE J	
C/O INTELLEVATE			ART UNIT	PAPER NUMBER
P.O. BOX 52050			2183	
MINNEAPOLIS, MN 55402				
SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE		DELIVERY MODE	
3 MONTHS	03/14/2007		PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/813,790	HONARY ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### **Status**

1) Responsive to communication(s) filed on 22 September 2006 and 08 January 2007.  
 2a) This action is **FINAL**.                            2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### **Disposition of Claims**

4) Claim(s) 1,2,4,5 and 7-24 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1,2,4,5 and 7-24 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### **Application Papers**

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 26 March 2004 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### **Priority under 35 U.S.C. § 119**

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### **Attachment(s)**

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____	6) <input type="checkbox"/> Other: _____

## **DETAILED ACTION**

1. Claims 1-2, 4-5, and 7-24 have been considered. Claims 3 and 6 have been cancelled as per Applicant's request. Claims 1, 10, 16, and 22 have been amended as per Applicant's request.

### ***Papers Submitted***

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as filed 22 September 2006; Extension of Time for 1 Month as filed 22 September 2006; and Amendment as filed 08 January 2007.

### ***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-2, 4-5, and 7-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The independent claims, taking claim 1 as exemplary, have the limitation "wherein said first process and said second process may be performed substantially in parallel." First, it is unclear whether the processes being performed in parallel is necessary to meet the claims due to the language "may be" in the limitation. The "may be" language suggests that the limitation is not necessary for the invention. Second, the meets and bounds of the claims are not clear due to the language "substantially in parallel." The "substantially" language is not clear as to whether the system performs in parallel or not, since it is unclear what "substantially" entails. The Examiner would point out that it is known in the art that, theoretically, parallel means that the operations are performed at the same time, but, in actual practice, the operations will not always happen at the same time, e.g. there is a slight time difference in the processes

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-24 are rejected under 35 U.S.C. 102(b) as being taught by Gove et al., U.S. Patent Number 5,212,777 (herein referred to as Gove). Examiner notes that, due to the lack of clarity in the claim language, the Examiner made assumptions with regards to the limitations rejected under 35 U.S.C. 112 second paragraphs above. The first assumption was that the processes are performed in parallel, and the second assumption was that “substantially” parallel constituted the processes happening at the same time.

7. Referring to claim 1, Gove has taught an apparatus, comprising:

- a. A memory unit to store data (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62);
- b. A plurality of parallel data paths to process said data (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62);

- c. A plurality of control units to control said data paths (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62); and
- d. A switch to connect said control units to said data paths, said switch to receive configuration information to establish a first set of connections between said control units and said data paths to execute a first process using single instruction multiple data processing, and a second set of connections between said control units and said data paths to execute a second process using multiple instruction multiple data processing(Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62);
- e. Wherein said first process and said second process may be performed substantially in parallel (Gove column 25, lines 44-54; column 63, lines 4-20; and column 170, lines 50-62).

8. Referring to claim 2, Gove has taught the apparatus of claim 1, wherein each control unit controls execution of a single program instruction (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column

9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62).

9. Referring to claim 4, Gove has taught the apparatus of claim 2, wherein said first set of connections connect at least one of said plurality of control units to multiple data paths, with said one control unit to control said multiple data paths (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62).

10. Referring to claim 5, Gove has taught the apparatus of claim 4, wherein each data path performs a same set of operations using said data (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62).

11. Referring to claim 7, Gove has taught the apparatus of claim 2, wherein said second set of connections connect multiple control units to multiple data paths, with each control unit to control a single data path (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62).

12. Referring to claim 8, Gove has taught the apparatus of claim 4, wherein each data path performs a different set of operations using said data (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to

column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62).

13. Referring to claim 9, Gove has taught the apparatus of claim 1, further comprising a configuration module to configure said switch to establish said connections in accordance with said configuration information (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62).

14. Referring to claim 10, Gove has taught a system, comprising:

- a. An antenna (Gove column 5, lines 49-56; column 28, lines 63-64; column 66, lines 3-8; and Figure 48). In regards to Gove, antennas send and receive signals for devices, such as televisions and remote cameras (Please see [www.dictionary.com "antenna"](http://www.dictionary.com/antenna) ©2000).
- b. A host processing system (Gove column 2, line 66 to column 3, line 4; column 5, lines 20-34; column 6, lines 23-36; column 12, line 63 to column 13, line 9; Figure 11 Figure 2; Figure 4; Figure 17; and Figure 29);
- c. A configuration module to store configuration information (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62); and

- d. A reconfigurable communication architecture module to receive said configuration information, said reconfigurable communication architecture module to configure itself to perform single instruction multiple data processing in a first configuration to execute a first process, and to perform multiple instruction multiple data processing in a second configuration to execute a second process (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62);
- e. Wherein said first process and said second process may be performed substantially in parallel (Gove column 25, lines 44-54; column 63, lines 4-20; and column 170, lines 50-62).

15. Referring to claim 11, Gove has taught the system of claim 10, wherein said

reconfiguration communication architecture module comprises:

- a. A plurality of processing elements to execute functions for each process (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62);
- b. A plurality of routing elements to connect said processing elements (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-

17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62); and

- c. A plurality of communications mediums to connects said processing elements and said routing elements in a mesh topology (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62). In regards to Gove, a “mesh topology” is where multiple nodes are connected together with multiple connections (Please see [www.its.blrdoc.gov](http://www.its.blrdoc.gov) “mesh topology” ©1996), which is shown in Gove’s Figures 4 and 17.

16. Referring to claim 12, Gove has taught the system of claim 10, wherein one of said processing elements comprises:

- a. A memory unit to store data (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62);
- b. A plurality of parallel data paths to process said data (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line

60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62);

- c. A plurality of control units to control said data paths (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62); and
- d. A switch to connect said control units to said data paths, said switch to receive said configuration information to establish a first set of connections between said control units and said data paths to execute said first process, and a second set of connections between said control units and said data paths to execute said second process (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62).

17. Referring to claim 13, Gove has taught the system of claim 12, wherein each control unit controls execution of a single program instruction (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62).

18. Referring to claim 14, Gove has taught the system of claim 13, wherein said first set of connections connect at least one of said plurality of control units to multiple data paths, with said

one control unit to control said multiple data paths (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62).

19. Referring to claim 15, Gove has taught the system of claim 13, wherein said second set of connections connect multiple control units to multiple data paths, with each control unit to control a single data path (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62).

20. Referring to claim 16, Gove has taught a method, comprising:

- a. Receiving configuration information at a switch (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62); and
- b. Configuring said switch to establish a first set of connections between a plurality of control units and a plurality of data paths to execute a first process using single instruction multiple data processing (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62,

line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62); and

- c. Configuring said switch to establish a second set of connections between said control units and said data paths to execute a second process using multiple instruction multiple data processing (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62);
- d. Wherein said first process and said second process may be performed substantially in parallel (Gove column 25, lines 44-54; column 63, lines 4-20; and column 170, lines 50-62).

21. Referring to claim 17, Gove has taught the method of claim 16, wherein each control unit controls execution of a single program instruction (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62).

22. Referring to claim 18, Gove has taught the method of claim 17, wherein said first set of connections connect at least one of said plurality of control units to multiple data paths, with said one control unit to control said multiple data paths (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column

9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62).

23. Referring to claim 19, Gove has taught the method of claim 17, wherein said second set of connections connect multiple control units to multiple data paths, with each control unit to control a single data path (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62).

24. Referring to claim 20, Gove has taught the method of claim 16, further comprising:

- a. Receiving a first set of data (Gove column 8, line 42 to column 9, line 13; column 10, lines 5-8, 22-29, and 38-44; column 10, line 65 to column 11, line 30; column 61, line 60 to column 62, line 24; Figure 12; Figure 13; Figure 14; Figure 15; Figure 61; and Figure 62)
- b. Storing said first set of data in a memory unit (Gove column 8, line 42 to column 9, line 13; column 10, lines 5-8, 22-29, and 38-44; column 10, line 65 to column 11, line 30; column 61, line 60 to column 62, line 24; Figure 12; Figure 13; Figure 14; Figure 15; Figure 61; and Figure 62); and
- c. Processing said first set of data with said data paths using said first set of connections (Gove column 8, line 42 to column 9, line 13; column 10, lines 5-8, 22-29, and 38-44; column 10, line 65 to column 11, line 30; column 61, line 60 to column 62, line 24; Figure 12; Figure 13; Figure 14; Figure 15; Figure 61; and Figure 62).

25. Referring to claim 21, Gove has taught the method of claim 16, further comprising:

- a. Receiving a second set of data (Gove column 8, line 42 to column 9, line 13; column 10, lines 5-8, 22-29, and 38-44; column 10, line 65 to column 11, line 30; column 61, line 60 to column 62, line 24; Figure 12; Figure 13; Figure 14; Figure 15; Figure 61; and Figure 62);
- b. Storing said second set of data in a memory unit (Gove column 8, line 42 to column 9, line 13; column 10, lines 5-8, 22-29, and 38-44; column 10, line 65 to column 11, line 30; column 61, line 60 to column 62, line 24; Figure 12; Figure 13; Figure 14; Figure 15; Figure 61; and Figure 62); and
- c. Processing said second set of data with said data paths using said second set of connections (Gove column 8, line 42 to column 9, line 13; column 10, lines 5-8, 22-29, and 38-44; column 10, line 65 to column 11, line 30; column 61, line 60 to column 62, line 24; Figure 12; Figure 13; Figure 14; Figure 15; Figure 61; and Figure 62).

26. Referring to claim 22, Gove has taught an article comprising:

- a. A storage medium (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62);
- b. Said storage medium including stored instructions that, when executed by a processor, result in receiving configuration information at a switch, configuring said switch to establish a first set of connections between a plurality of control

units and a plurality of data paths to execute a first process using single instruction multiple data processing, and configuring said switch to establish a second set of connections between said control units and said data paths to execute a second process using multiple instruction multiple data processing (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62);

- c. Wherein said first process and said second process may be performed substantially in parallel (Gove column 25, lines 44-54; column 63, lines 4-20; and column 170, lines 50-62).

27. Referring to claim 23, Gove has taught the article of claim 22, wherein the stored instructions, when executed by a processor, further result in said first set of connections connecting at least one of said plurality of control units to multiple data paths, with said one control unit to control said multiple data paths (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62).

28. Referring to claim 24, Gove has taught the article of claim 22, wherein the stored instructions, when executed by a processor, further result in said second set of connections connecting multiple control units to multiple data paths, with each control unit to control a single data path (Gove column 1, line 47 to column 3, line 20; column 5, lines 20-56; column 6, lines 6-

43; column 7, lines 5-13; column 8, line 42 to column 9, line 13; column 16, lines 6-17; column 61, line 60 to column 62, line 24; Figure 1; Figure 2; Figure 4; Figure 14; Figure 15; Figure 17; Figure 61; and Figure 62).

***Response to Arguments***

29. Examiner withdraws objections to the Specification in favor of the amended Specification.
30. Applicants argue in essence on pages 10-13

...Applicant respectfully submits that the Gove reference arguably teaches a system that can “switch between operational modes” as necessary, however, the Gove reference fails to teach, suggest or disclose a system wherein the different operational modes can be performed substantially in parallel. Consequently, the Gove reference fails to disclose all the elements or features of the claimed subject matter...
31. This has not been found persuasive. Gove teaches in column 26, lines 44-54

...This register contains bits which indicated whether the system is MIMD, SIMD, or some combination (hybrid) of SIMD and MIMD...While the embodiment shows one pair of signals, in actual practice an individual pair of signals for each processor could be supplied...
32. This means that a portion of Gove’s processors is in SIMD mode and executing SIMD operations, while the other portion is in MIMD mode executing MIMD operations. Therefore, the SIMD process and the MIMD process are performed in parallel. This is further supports in Gove in column 63, lines 4-20 by stating “...changing at least some of the processors from

operation in the SIMD operating mode to operation in the MIMD operational mode..." suggesting that not all of the processors are necessarily changed from a SIMD mode operating on the same instruction to a MIMD mode operating on separate instructions. Gove also claims this feature in his claim 8 with the limitation

wherein some of said plurality of processors may operate in the multiple instruction multiple data (MIMD) mode and while serial chains of processors operate in the single instruction multiple data (SIMD) mode, said instruction port of each processor in a serial chain of processors in the single instruction multiple data (SIMD) mode being connected to said instruction memory corresponding to a first processor in the serial chain, and said instruction port of each processor in the multiple instruction multiple data (MIMD) mode being connected to said corresponding instruction memory.

### *Conclusion*

33. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- a. Barker et al., U.S. Patent Number 5,625,836 A, has taught a SIMD-MIMD system where SIMD and MIMD operations can operate in parallel.
- b. Wilkinson et al., U.S. Patent Numbers 5,754,871 A; 5,828,894 A; 5,761,523 A; 5,966,528 A; and 6,094,715 A, have taught a parallel processing system that allows SIMD and MIMD operations to operate in parallel.
- c. Dapp et al., U.S. Patent Number 5,734,921 A, has taught a SIMD and MIMD combination system.

- d. Pechanek et al., U.S. Patent Numbers 6,151,668 A and 6,446,191 B1, have taught combination SIMD and MIMD systems.
- e. Barry et al., U.S. Patent Numbers 6,167,501 A; 6,366,997 B1; and 6,795,909 B2, have taught hybrid SIMD and MIMD systems.

34. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

35. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

37. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

38. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Aimee J. Li  
10 March 2007

*Eddie Chan*  
EDDIE CHAN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER, 2100